CLAIMS

What is claimed is:

1. An electrically alterable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, and a first channel region defined between the first diffusion region and the second diffusion region;

a first floating gate having a first height and comprised of a conductive material, the first floating gate disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the first floating gate capable of storing electrical charge;

a second floating gate having a second height and comprised of a conductive material, the second floating gate disposed adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region, the second floating gate capable of storing electrical charge; and

a control gate having a third height and comprised of a conductive material, the control gate disposed laterally between the first floating gate and the second floating gate, the control gate separated from the first floating gate by a first vertical insulator layer and separated from the second floating gate by a second vertical insulator layer, the control

gate further being above the first channel region and separated therefrom by a third insulator region.

2. The memory device of claim 1, wherein the first dopant having a P-type characteristic and the second dopant having an N-type characteristic.

3. The memory device of claim 1, wherein the first dopant having an N-type characteristic and the second dopant having a P-type characteristic.

4. The memory device of claim 1, wherein the first insulator region having a thickness that allows tunneling of charge between the first floating gate and the first channel region.

5. The memory device of claim 4, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

6. The memory device of claim 1, wherein the third insulator region having a thickness that allows tunneling of charge between the second floating gate and the first channel region.

7. The memory device of claim 6, wherein the thickness of the third insulator region is between 70 Angstroms and 110 Angstroms.

8. The memory device of claim 1, wherein the first vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the first floating gate and the control gate, and the first vertical insulator preventing leakage between the first floating gate and the control gate.

9. The memory device of claim 1, wherein the first vertical insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the first

floating gate and the control gate, and the first vertical insulator prevents leakage between the first floating gate and the control gate.

10. The memory device of claim 1, wherein the first vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the second floating gate and the control gate, and the first vertical insulator preventing leakage between the second floating gate and the control gate.

11. The memory device of claim 1, wherein the second vertical insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the second floating gate and the control gate, and the second vertical insulator preventing leakage between the second floating gate and the control gate.

12. The memory device of claim 1, wherein the first height of the first floating gate is taller than the third height.

13. The memory device of claim 1, wherein the first height of the first floating gate is shorter than the third height.

14. The memory device of claim 1, wherein the first height of the first floating gate is same as the third height.

15. The memory device of claim 1, wherein the first floating gate and the second floating gate each being capable of storing multiple levels of charge.

16. The memory device of claim 1, wherein the first floating gate and the second floating gate each being capable of storing four levels of charge.

17. The memory device of claim 1, wherein an oxidation layer is disposed on top of each diffusion region.

18. The memory device of claim 1, wherein a charge is transported from the first channel region to the second floating gate when a first combination of voltages is applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

19. The memory device of claim 18 wherein the first combination of voltages comprises:

applying a zero voltage to the second semiconductor layer;

applying a positive high voltage to the first diffusion region;

applying a zero voltage to the second diffusion region; and

applying a positive high voltage to the control gate.

20. The memory device of claim 18, wherein the first combination of voltages comprises:

applying a positive high ramp down voltage followed by a ramp up voltage to the control gate;

applying a positive high voltage to the first diffusion region;

applying a zero voltage to the second diffusion region; and

applying a positive high voltage to the second semiconductor layer.

21. The memory device of claim 18 wherein the first combination of voltages comprises:

applying a Vcc voltage to the second semiconductor layer;

applying a negative voltage to the second diffusion region; and

applying a positive high voltage to the control gate.

22. The memory device of claim 1, wherein charge inside the second floating gate can be determined when a second combination of voltages is applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

23. The memory device of claim 22, wherein the second combination of voltages comprises:

applying a zero voltage to the second semiconductor layer;

applying a voltage between 0V and Vcc voltage to the first diffusion region; and

applying a voltage between 0V and Vcc to the control gate.

24. The memory device of claim 22, wherein the second combination of voltages comprises:

applying a Vcc voltage to the second semiconductor layer;

applying a voltage between 0v and Vcc to the first diffusion region;

applying a Vcc voltage to the second diffusion region; and

applying a voltage between 0V and Vcc voltage to the control gate.

25. The memory device of claim 1, wherein charge is removed from the second floating gate when a third combination of voltages is applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

26. The memory device of claim 25, wherein the third combination of voltages comprises:

applying a negative voltage to the control gate; and

applying a positive high voltage to the second semiconductor layer.

27. An electrically alterable non-volatile memory string comprising:

a plurality of memory devices, each memory device having a control transistor capable of storing a plurality of data, the plurality of memory devices having a first end and a second end;

a first select transistor connected to the first end;

a second select transistor connected to the second end; and

a connector connecting the first select transistor to a bit line.

28. The memory string of claim 27, wherein the first select transistor being further connected to the second select transistor of an adjacent memory string.

29. The memory string of claim 27, wherein the control transistor being capable of storing data representing four logic states.

30. The memory string of claim 27, wherein the control transistor being capable of storing data representing multiple logic states

31. The memory string of claim 27, one memory device being connected to an adjacent memory device, whereby a drain of one memory device being connected to a source of an adjacent device.

32. An electrically alterable non-volatile memory string comprising:

a plurality of memory devices, each memory device having a control transistor capable of storing a plurality of data, each memory device having a first end and a second end;

a first diffusion region connected to the first end of each memory device;

a second diffusion region, spaced-apart from the first diffusion region, connected to the second end of each memory device; and

a plurality of connectors connecting the control transistor of each memory device to a bit line.

33. The memory string of claim 32, wherein the control transistor being capable of storing data representing four logic states.

34. The memory string of claim 32, wherein the control transistor being capable of storing data representing multiple logic states

35. The memory string of claim 32, wherein the memory devices are connected in parallel to each other between the first diffusion region and the second diffusion region.

36. An electrically alterable, non-volatile memory array, comprising:

a plurality of memory strings, each memory string having

a first connector connected to a drain of a first select transistor in the memory string,

a second connector connected to a gate of the first select transistor,

a third connector connected to a gate of a memory cell transistor in the memory string, and

a fourth connector connected to a gate of a second select transistor in the memory string, wherein the plurality of memory strings are arranged in such way that the drain of the first select transistor in a first memory string is connected to a source of the second select transistor in an adjacent second memory string;

a plurality of bit lines, wherein each bit line being connected to the first connector of every memory string;

a plurality of first select lines, wherein each first select line being connected to the second connector of every memory string;

a plurality of control lines, where each control line being connected to the third connector of every memory string; and

a plurality of second select lines, wherein each second select line being connected to the fourth connector of every memory string.

37. The memory array of claim 36, wherein the memory cell transistor of one memory string is separated from a memory cell transistor of adjacent memory string by an isolation layer.

38. The memory array of claim 37, wherein the isolation layer is a shallow trench isolation.